REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 19-38 are pending in the present application. Claims 19, 32, 35, 36, and 38 are amended by the present amendment.

In the outstanding Office Action, Claims 19-38 were rejected under 35 U.S.C. § 103(a) as unpatentable over Steely, Jr. et al. (U.S. Patent No. 6,088,771, herein "Steely") in view of Dieffenderfer et al. (U.S. Patent No. 5,822,608, herein "Dieffenderfer"), which is respectfully traversed for the following reasons.

Independent Claims 19, 32, 35, 36, and 38 have been amended to more clearly recite that a request sent to a state element includes a command that directs the state element on how to perform on a shared state. These claim amendments find support in the specification, for example, at page 7, second full paragraph. In addition, the independent claims have been amended to recite that a memory is connected to the state element and configured to store the shared state. These claim amendments find support, for example, in Figure 6 and its corresponding description in the specification. In addition, the abstract has been amended to be consistent with the amended claims. No new matter has been added.

Briefly recapitulating, independent Claim 19 is directed to a state engine that receives multiple requests from a parallel processor for a shared state. The state

engine includes at least one state element means, the at least one state element means adapted to operate, atomically, on the shared state in response to a request made by the parallel processor. The request includes at least a command directing the at least one state element means on how to perform an operation on the shared state. The state engine also includes a memory connected to the at least one state element means and configured to store the shared state.

The claimed one state element unit advantageously achieves faster access for the parallel processor to the shared state, as shown for example in Figure 5(b) and its corresponding description in the specification.

Turning to the applied art, Steely discloses a technique that reduces a latency of a memory barrier operation used to impose an inter-reference order between sets of memory reference operations issued by a processor to a multiprocessor system having a shared memory. More specifically, Figure 2 shows a local switch 200 communicating with a plurality of processors P1 to P4 such that inputs from the processors are serialized before being sent to a shared memory 150. Figure 2 shows that the switch 200 includes an arbiter 240 that arbitrates, among input queues from the processors P1 to P4, to grant access to the Arb bus 170, where the requests are ordered into a memory reference request stream. The arbiter 240 selects the request stored in the input queues for access to the bus in accordance with an arbitration policy, such as a conventional round-robin algorithm, as disclosed in Steely in the paragraph bridging columns 6 and 7.

Thus, the device of Steely does not teach or suggest that a request from any of the processors P1 to P4 includes at least a command directing the arbiter 240 on how to perform an operation on the shared memory 150, as recited by the independent Claims.

In other words, the arbitration system of Steely does not perform an operation on the shared memory 150 based on a command from the processors P1 to P4 but rather acts based on the round-robin algorithm, which is not provided by the processors P1 to P4. Steely simply queues and arbitrates updates to memory from the processors and does not teach or suggest processors sending commands to the state engine directing it on how to update the memory.

In this regard, if a processor in Steely needs to increment a shared memory location, then the processor needs to read the data from the memory, increment the value, write it back to the memory, and then issue a memory barrier instruction to synchronize this update with all the other processes. However, this operation delays the other processors from accessing that memory location until the first processor has finished the complete sequence read-modify-write operation, as illustrated in Figure 5(b).

To the contrary, the claimed invention avoids this latency because any number of state processors may instruct the state engine via the requests, for example, to increment the same shared state and the processors may immediately continue with

other processing. Thus, the processors do not have to wait for the whole operation read-modify-write to be performed, as illustrated by Figure 5(a).

In addition, the independent claims recite that the state engine also includes a memory connected to the at least one state element means and configured to store the shared state. Steely is silent about a memory that stores the shared state being included in the switch 200. On the contrary, Figure 2 of Steely clearly shows that the memory 150 that stores the shared state is outside the switch 200.

Therefore, Applicant respectfully submits that Steely is lacking not only the request made by the parallel processor, as acknowledged by the outstanding Office Action at page 3, second full paragraph, but also a request that includes at least a command directing at least one state element means on how to perform an operation on a shared state, and a memory connected to the at least one state element means and configured to store the shared state.

Dieffenderfer has been considered but does not cure the deficiencies of Steely discussed above with regard to independent Claim 19.

Accordingly, it is respectfully submitted that independent Claims 19, 32, 35, 36, and 38 and each of the claims depending therefrom patentably distinguish over Steely and Dieffenderfer, either alone or in combination.

All of the objections and rejections raised in the outstanding Office Action having been addressed, it is respectfully submitted that this application is in condition for allowance and a notice to that effect is earnestly solicited. Should the Examiner have any questions regarding this response or the application in general, she or he is invited to contact the undersigned at (540) 361-2601.

Respectfully submitted,

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